REMARKS

By the present Amendment, Applicants have amended claims 14, 18, 22, and 27 to more appropriately define the present invention. Claims 14-33 are pending.

In the Office Action, the Examiner rejected claims 14-33 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement; rejected claims 14-31 under 35 U.S.C. § 103(a) as being unpatentable over Shin (U.S. Patent No. 5,270,257) further in view of Kirvokapic (U.S. Patent No. 6,025,635); and rejected claims 32-33 under 35 U.S.C. § 103(a) as being unpatentable over Shin and Kirvokapic and further in view of Lee (U.S. Patent No. 6,228,763).

Applicants respectfully traverse each of the rejections as set forth above based on the following remarks:

Rejection under 35 U.S.C. § 112, first paragraph

On pages 2-3 of the Office Action, the Examiner rejected claims 14-33 under 35 U.S.C. § 112, first paragraph, alleging that claims 14,18, 22, and 27 contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. Specifically, the Examiner alleges that claims 14, 18, 22, and 27 recite "removing said second film to form a second groove in the semiconductor substrate," which is not described in the specification or the drawings. Office Action at pages 2-3. Applicants respectfully disagree.

Present independent claims 14 and 18 recite a method for producing a MIS transistor comprising, among other things, "forming an insulator film on said impurity diffusion region and thereafter removing said second film to form a second groove on the semiconductor substrate so that a top surface of the impurity diffusion region of the

semiconductor substrate is higher than a bottom surface of the second groove." This is clearly supported by the originally-filed application, for example, at least Figs. 3A - 3E and page 12 of the Specification and Figs. 4A - 4E and pages 12-14 of the Specification.

Furthermore, present independent claim 22 recites "removing said first film so as to form a groove on the semiconductor substrate; forming a gate insulator in said groove on the semiconductor substrate with controlling a thickness of the gate insulator film so that a top surface of said gate insulator film is higher than a top surface of said impurity diffusion region" and claim 27 recites "etching said high dielectric film so as to form said gate insulator film by using said gate electrode and side walls as a mask and forming a side wall insulator film at a side of said gate insulator film; and diffusing an impurity on a surface of said semiconductor substrate to form an impurity diffusion region including an elevated impurity diffusion region from a channel region with controlling a thickness of elevated impurity region by using said gate insulator film as a mask, so that a top surface of the gate insulator film is higher than a top surface of the elevated impurity region and that said top surface of the elevated impurity region is higher than a top surface of said channel region of the semiconductor substrate." Each of these recitations is clearly supported by the originally-filed application, for example, at least Figs. 6A-6E and pages 15-16 of the Specification and Figs. 9A-9E and pages 17-18 of the Specification, respectively.

Therefore, Applicants respectfully submit, each of the independent claims 14, 18, 22, and 27, and claims 15-17, 19-21, 23-26, and 28-31 that depend therefrom are supported by the originally-filed application. Furthermore, claims 32-33 do not contain a

recitation of "a groove in a semiconductor substrate" and the Examiner has not stated any reason for a rejection of claims 32-33 under 35 U.S.C. § 112, first paragraph. Therefore, the rejection of claims 32-33 under 35 U.S.C. § 112, first paragraph is improper. Accordingly, Applicants request the Examiner to withdraw the rejection of claims 14-33 under 35 U.S.C. § 112, first paragraph, and the claims allowed.

In making various references to the Specification and drawings set forth herein, it is to be understood that Applicants are in no way intending to limit the scope of the claims to the exemplary embodiments shown in the drawings and described in the Specification. Rather, Applicants expressly affirm that they are entitled to have the claims interpreted broadly, to the maximum extent permitted by statute, regulation, and applicable case law.

Rejection under 35 U.S.C. § 103

In the Office Action, the Examiner rejected claims 14-31 under 35 U.S.C. § 103(a) as being unpatentable over Shin (U.S. Patent No. 5,270,257) further in view of Kirvokapic (U.S. Patent No. 6,025,635); and rejected claims 32-33 under 35 U.S.C. § 103(a) as being unpatentable over Shin, Kirvokapic, and Lee.

Regarding the rejection of claims 14-33 under 35 U.S.C. § 103(a), Applicants respectfully disagree with the Examiner's arguments and conclusions as set forth in the Office Action.

To establish a *prima facie* case of obviousness under 35 U.S.C. §103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element recited in the claims. (See M.P.E.P. §2143.03 (8th ed. 2001)). Second, there must be some suggestion or

motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must "be found in the prior art, and not be based on applicant's disclosure." (M.P.E.P. §2143 (8th ed. 2001)).

I. Claims 14 and 18

The Examiner's rejection of claims 14 and 18 under § 103 fails to meet the essential requirements for a *prima facie* case of obviousness, as set forth below.

Claims 14 and 18 recite a method for producing a MIS transistor comprising, *inter alia*, "forming an insulator film on said impurity diffusion region and thereafter removing said second film to form a second groove on the semiconductor substrate so that a top surface of the impurity diffusion region of the semiconductor substrate is higher than a bottom surface of the second groove."

added by the amendment

In contrast, Shin discloses in Figs. 3a and 3b forming a nitride layer 22 on a substrate 21, etching a portion of the nitride layer 22 to form a mask, and then etching the substrate 21 to form a trench (col. 4, lines 15-27). Fig. 3b further shows a gate oxide layer 23 is grown on the exposed trench surface of the substrate 21 and the nitride layer 22 (col. 4, lines 30-32). A polysilicon gate 24 is formed in the trench, and the silicon substrate 21 is doped to form source 26a and drain 26b (Fig. 3b, col. 4, lines 40-47).

Fig. 3b of Shin shows a gate oxide layer 23, which is grown on the exposed trench surface of the substrate; however, Shin does not teach or suggest at least "forming an insulator film on said impurity diffusion region and thereafter removing said

second film to form a second groove on the semiconductor substrate so that a top surface of the impurity diffusion region of the semiconductor substrate is higher than a bottom surface of the second groove," as recited in claims 14 and 18. In fact, the gate oxide film 23 (alleged by the Examiner to read on the claimed "second film") is not removed at all. Furthermore, nothing in Shin discloses forming a second groove, or a "second groove on the semiconductor substrate," as recited in claims 14 and 18.

Therefore, Shin does not teach or suggest all the elements of claims 14 and 18, for example, "forming an insulator film on said impurity diffusion region and thereafter removing said second film to form a second groove on the semiconductor substrate so that a top surface of the impurity diffusion region of the semiconductor substrate is higher than a bottom surface of the second groove," as recited in claims 14 and 18.

Krivokapic does not cure the deficiencies of Shin noted above. In the "Response to Arguments" section of the Office Action, the Examiner points to Fig. 9 and elements 200a to allege that Krivokapic "shows formation of an insulation film (215) on an impurity diffusion region (fig. 9) and thereafter removing a second film (205) to form a second groove (fig. 9, 200a) in the semiconductor substrate (it is noted that the phrase 'in the semiconductor substrate' is new matter)." Office Action at page 8. Contrary to the allegations of the Examiner, Figs. 8, 9, and 15 of Krivokapic do not teach or suggest at least "forming an insulator film on said impurity diffusion region and thereafter removing said second film to form a second groove on the semiconductor substrate so that a top surface of the impurity diffusion region of the semiconductor substrate is higher than a bottom surface of the second groove," as recited in claims 14 and 18.

added by amendment

Fig. 8 of Krivokapic discloses forming adaptively controlled spacers 215 in gate region 190 (col. 6, lines 19-21) by depositing Si_3N_4 and isotopically etching the Si_3N_4 layer to yield spacers 215. Id. at col. 6, lines 19-24. Fig. 9 discloses etching oxide layer 200 to leave a minor portion of the oxide layer 200a under spacers 215 for support. Id. at col. 6, lines 28-34.

First, while Krivokapic discloses etching oxide layer 200 to leave a minor portion 200a under spacers for support, this does not constitute at least "forming an insulator film on said impurity diffusion region and thereafter removing said second film to form a second groove on the semiconductor substrate *so that a top surface of the impurity diffusion region of the semiconductor substrate is higher than a bottom surface of the second groove,*" as claimed. (Emphasis added). The "second groove" of Kirvokapic is formed on top of the substrate 60. See Figs. 8 and 9. Second, Figs. 8 and 9 of Krivokapic do not disclose that the oxide layer 200 is formed "*on [an] impurity region,*" as recited in claims 14 and 18.

Fig. 13 of Krivokapic discloses the device after formation of a source and drain region, which are formed by a deposition or implantation of an impurity. Id. at col. 7, lines 7-12. While Fig. 15 of Krivokapic discloses a film 232 on an impurity region 200a, film 232 is NOT removed. Therefore, in reference to film 232, Krivokapic does not disclose the step of "forming an insulator film on said impurity diffusion region and thereafter removing said second film to form a second groove on the semiconductor substrate *so that a top surface of the impurity diffusion region of the semiconductor substrate is higher than a bottom surface of the second groove,*" as recited in claims 14 and 18.

Thus, neither the film 200 nor the film 232 (nor any other film) of Krivokapic cure the deficiencies of Shin. To summarize Shin and Kirvokapic, either taken alone *or in combination*, do not teach or suggest at least "forming an insulator film on said impurity diffusion region and thereafter removing said second film to form a second groove on the semiconductor substrate so that a top surface of the impurity diffusion region of the semiconductor substrate is higher than a bottom surface of the second groove," as recited in claims 14 and 18. Likewise, there is lack of any reasonable expectation of success from combining the references.

Furthermore, claim 14 recites, among other things, "forming a gate insulator film in said second groove with controlling a thickness of the gate insulator film so that a top surface of said gate insulator film is higher than a top surface of said impurity diffusion region." Shin does not teach or suggest any second groove. Therefore, Shin necessarily also does not teach or suggest "forming a gate insulator film in said second groove with controlling a thickness of the gate insulator film so that a top surface of said gate insulator film is higher than a top surface of said impurity diffusion region," as recited in claim 14. Further, Kirvokapic also fails to teach or suggest this claimed step. Therefore, Shin and Kirvokapic, either taken alone or in combination, fail to teach or suggest at least this claimed step.

Moreover, claim 18 recites, among other things, "polishing said gate insulator film by using said insulator film as a stopper with controlling a thickness of the gate insulator film so that a top surface of said gate insulator film is higher than a top surface of said impurity diffusion region." As discussed above, in view of no teaching or suggestion in Shin regarding a second groove, Shin does not teach or suggest at least this claimed

step. Furthermore, Kirvokapic also fails to teach or suggest this claimed step. Therefore, Shin and Kirvokapic, either taken alone or in combination, fail to teach or suggest at least this claimed step.

Further, Applicants respectfully disagree with the Examiner's alleged reasons for combining the teachings of Shin with those of Kirvokapic. Even if a motivation stemming from an alleged general desire to make more efficient devices were a sufficient reason to combine references (which it is not), it is improper to rely on such general motivation to pick and choose, at random, elements from one reference to cure the deficiencies of another reference. Without appropriate particularized motivation from the references themselves or from knowledge generally known in the art to combine specific elements of one reference with the elements of another reference, the Examiner is, in effect, ignoring the Applicants' invention by inappropriately using the present application's own teachings as motivation to modify the cited references. To do this, constitutes impermissible hindsight based on Applicants' disclosure.

To summarize, the Examiner has failed to make a *prima facie* case of obviousness at least because Shin and Krivokapic, either taken alone or in combination, do not teach each and every element of claims 14 and 18. Therefore, Applicants respectfully request that the Examiner withdraw the rejection of claims 14 and 18 under 35 U.S.C. § 103(a), and allow these claims.

Claims 15-17 and 19-21 depend from claim 14 and 18, respectively. Accordingly, these claims are allowable as well at least in view of their dependency from allowable claims 14 and 18.

I. Claims 22 and 27

The Examiner's rejection of claims 22 and 27 under § 103 fails to meet the essential requirements for a *prima facie* case of obviousness, as set forth below.

Claim 22 recites a method for producing a MIS transistor comprising, *inter alia*, "forming an insulator film on said impurity diffusion region so that a top surface of the impurity diffusion region of the semiconductor substrate is higher than an upper level of the channel region; removing said first film so as to form a groove on the semiconductor substrate; and forming a gate insulator in said groove on the semiconductor substrate with controlling a thickness of the gate insulator film so that a top surface of said gate insulator film is higher than a top surface of said impurity diffusion region."

In the "Response to Arguments" section of the Office Action, the Examiner states that Applicants' previous arguments were not persuasive because "[S]hin in figures 3b to 3e shows layer (23/25/27) all within the substrate." Office Action at page 10. Applicants respectfully disagree.

As shown in Fig. 3c of Shin, a bottom surface of source 26a and drain 26b is higher than the bottom surface of the trench. Fig. 3b further shows a gate oxide layer 23 is grown on the exposed trench surface of the substrate 21 As is clear from Figs. 3b and 3c, to the extent source 26a or drain 26b may correspond to the impurity diffusion region, Shin does not teach or suggest at least "forming an insulator film on said impurity diffusion region so that a top surface of the impurity diffusion region of the semiconductor substrate is higher than an upper level of the channel region; removing said first film so as to form a groove on the semiconductor substrate; and forming a gate insulator in said groove on the semiconductor substrate with controlling a thickness of

the gate insulator film so that a top surface of said gate insulator film is higher than a top surface of said impurity diffusion region," as recited in claim 22.

Krivokapic fails to cure the above-mentioned deficiencies of Shin. As mentioned before with respect to claims 14 and 18, Fig. 15 of Krivokapic discloses a film 232 on an impurity region 200a. However, Krivokapic does not teach or suggest at least "forming an insulator film on said impurity diffusion region so that a top surface of the impurity diffusion region of the semiconductor substrate is higher than an upper level of the channel region; removing said first film so as to form a groove on the semiconductor substrate; and forming a gate insulator in said groove on the semiconductor substrate with controlling a thickness of the gate insulator film so that a top surface of said gate insulator film is higher than a top surface of said impurity diffusion region," as recited in claim 22.

Therefore, Shin and Kirvokapic, either taken alone or in combination, do not teach or suggest at least "forming an insulator film on said impurity diffusion region so that a top surface of the impurity diffusion region of the semiconductor substrate is higher than an upper level of the channel region; removing said first film so as to form a groove on the semiconductor substrate; and forming a gate insulator in said groove on the semiconductor substrate with controlling a thickness of the gate insulator film so that a top surface of said gate insulator film is higher than a top surface of said impurity diffusion region," as recited in claim 22.

Claim 27 recites a method for producing a MIS transistor comprising, *inter alia*, "forming a high dielectric film to be a gate insulator film on said semiconductor substrate; sequentially depositing a laminated film on said high dielectric film by a

polycrystalline semiconductor film to be a gate electrode; etching said laminated film so as to form said gate electrode and thereafter forming side walls at a side of said gate electrode; etching said high dielectric film so as to form said gate insulator film by using said gate electrode and side walls as a mask and forming a side wall insulator film at a side of said gate insulator film; and diffusing an impurity on a surface of said semiconductor substrate to form an impurity diffusion region including an elevated impurity diffusion region from a channel region with controlling a thickness of elevated impurity region by using said gate insulator film as a mask, so that a top surface of the gate insulator film is higher than a top surface of the elevated impurity region and that said top surface of the elevated impurity region is higher than a top surface of said channel region of the semiconductor substrate." Neither Shin nor Kirvokapic, either taken alone or in combination, teach or suggest at least this element of claim 27.

Accordingly, the Examiner has failed to make a *prima facie* case of obviousness for claims 22 and 27. Applicants respectfully request the Examiner to withdraw the rejection of claims 22 and 27 under 35 U.S.C. § 103(a), and to allow claims 22 and 27.

Claims 23-26 and 28-31 depend from claim 22 and 27, respectively. Accordingly, these claims are allowable as well at least in view of their dependency from allowable claims 22 and 27.

III. Claim 32

Claim 32 recites a method for producing a MIS transistor comprising, *inter alia*, "selectively depositing semiconductor layers serving as said source/drain regions so that an inclined surface is formed between the top surface of said semiconductor

substrate and said channel region." None of the cited references disclose or suggest at least this element of claim 32.

In the "Response to Arguments" section of the Office Action, the Examiner points to elements 26a and 26b of Fig 3e in Shin to allege that it discloses the above-quoted elements of claim 32. However, Shin does not disclose any inclined surface between the top surface of the semiconductor substrate and a channel region. In fact, the inclined surface 26a and 26b in Shin is not formed between the top surface of semiconductor substrate and channel region, as required by claim 32.

Lee, cited only for the T-shaped cross-section, does not cure the deficiencies of the Shin and Kirvokapic combination. Therefore, Shin, Kirvokapic, and Lee, either taken alone or in combination, do not teach or suggest at least "selectively depositing semiconductor layers serving as said source/drain regions so that an inclined surface is formed between the top surface of said semiconductor substrate and said channel region," as recited in claim 32.

Therefore, the Examiner has failed to make a *prima facie* case of obviousness for claim 32 and Applicants respectfully request the Examiner to withdraw the rejection of claim 32 under 35 U.S.C. § 103(a), and to allow claim 32.

Claim 33 depends from claim 32. Accordingly, claim 32 is also allowable at least in view of its dependency from allowable claim 32.

Conclusion

In view of the foregoing remarks, Applicants respectfully request reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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